


REMARKS

Claims 1-3 and 8 have been amended to further distinguish the present invention over the prior art of record and new claims 76-99 have been added to recite additional protection to which Applicant is entitled. The present application is believed to be in condition for allowance and favorable consideration is requested.

Examination on the merits is requested.

Respectfully submitted,


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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1.(Twice Amended) An active matrix type display device comprising:

at least two transistors provided on an insulating surface in a [XY-branching] buffer circuit [of a peripheral circuit of] in said active matrix type display device;

a common gate wiring provided [on] over said insulating surface and connected with said at least two transistors at gate electrodes of said at least two transistors;

a common source wiring provided [on] over said insulating surface and connected with said at least two transistors at one of source and drain of each of said at least two transistors;

a common drain wiring provided [on] over said insulating surface and connected with said at least two transistors at the other of the source and drain of each of said at least two transistors,

wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring, and said common drain wiring with said at least two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate [islands] semiconductor layers respectively, each of said channel-forming regions containing carbon and nitrogen at a concentration of $5 \times 10^{18} \text{ cm}^{-3}$ or less, respectively, and containing oxygen at a concentration of $5 \times 10^{19} \text{ cm}^{-3}$ or less.

2.(Twice Amended) An active matrix type display device comprising:

at least two transistors provided on an insulating surface in [a decoder circuit of] a driver circuit [of] in said active matrix type display device;

a common gate wiring provided [on] over said insulating surface and connected with said at least two transistors at gate electrodes of said at least two transistors;

a common source wiring provided [on] over said insulating surface and connected with said at least two transistors at one of source and drain of each of said at least two transistors; and

a common drain wiring provided [on] over said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring, and said common drain wiring with said at least two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate [islands] semiconductor layers respectively, each of said channel-forming regions containing carbon and nitrogen at a concentration of $5 \times 10^{18} \text{ cm}^{-3}$ or less, respectively, and containing oxygen at a concentration of $5 \times 10^{19} \text{ cm}^{-3}$ or less.

3.(Twice Amended) An active matrix type display device comprising:

at least two transistors provided on an insulating surface in a buffer circuit [of a driver circuit of] in said active matrix type display device;

a common gate wiring provided [on] over said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided [on] over said insulating surface and connected with said at least two transistors at one of source and drain of each of said at least two transistors; and

a common drain wiring provided [on] over said insulating surface and connected with said at least two transistors at the other of the source and drain of each of said at least two transistors,

wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring, and said common drain wiring with said at least two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate [islands] semiconductor layers respectively, each of said channel-forming regions containing carbon and nitrogen at a concentration of $5 \times 10^{18} \text{ cm}^{-3}$ or less, respectively, and containing oxygen at a concentration of $5 \times 10^{19} \text{ cm}^{-3}$ or less, and each of said channel-forming regions not having linear defects or surface defects.

8.(Twice Amended) An active matrix type display device comprising:

at least two transistors provided on an insulating surface in a driver circuit [of] in said active matrix type display device;

a common gate wiring provided on said insulating surface and connected with said at least two transistors at gate electrodes of said at least two transistors;

a common source wiring provided on said insulating surface and connected with said at least two transistors at one of source and drain of each of said at least two transistors; and

a common drain wiring provided on said insulating surface and connected with said at least two transistors at the other of the source and drain of each of said at least two transistors,

wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said at least two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate [islands] semiconductor layers respectively, each of said channel-forming regions containing carbon and nitrogen at a concentration of $5 \times 10^{18} \text{ cm}^{-3}$ or less, respectively, and containing oxygen at a

concentration of $5 \times 10^{19} \text{ cm}^{-3}$ or less, and each of said channel-forming regions not having linear defects or surface defects.